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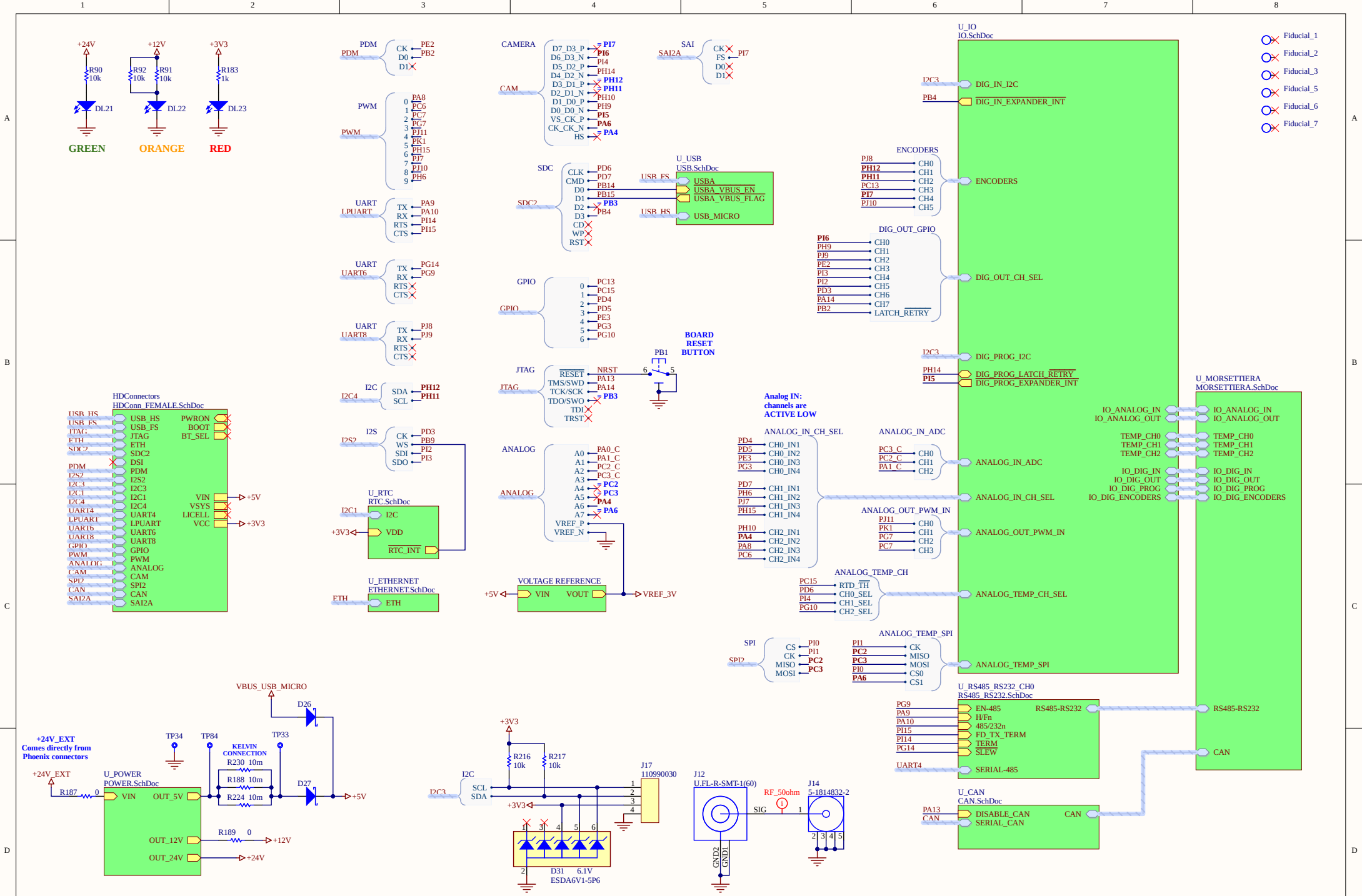
D

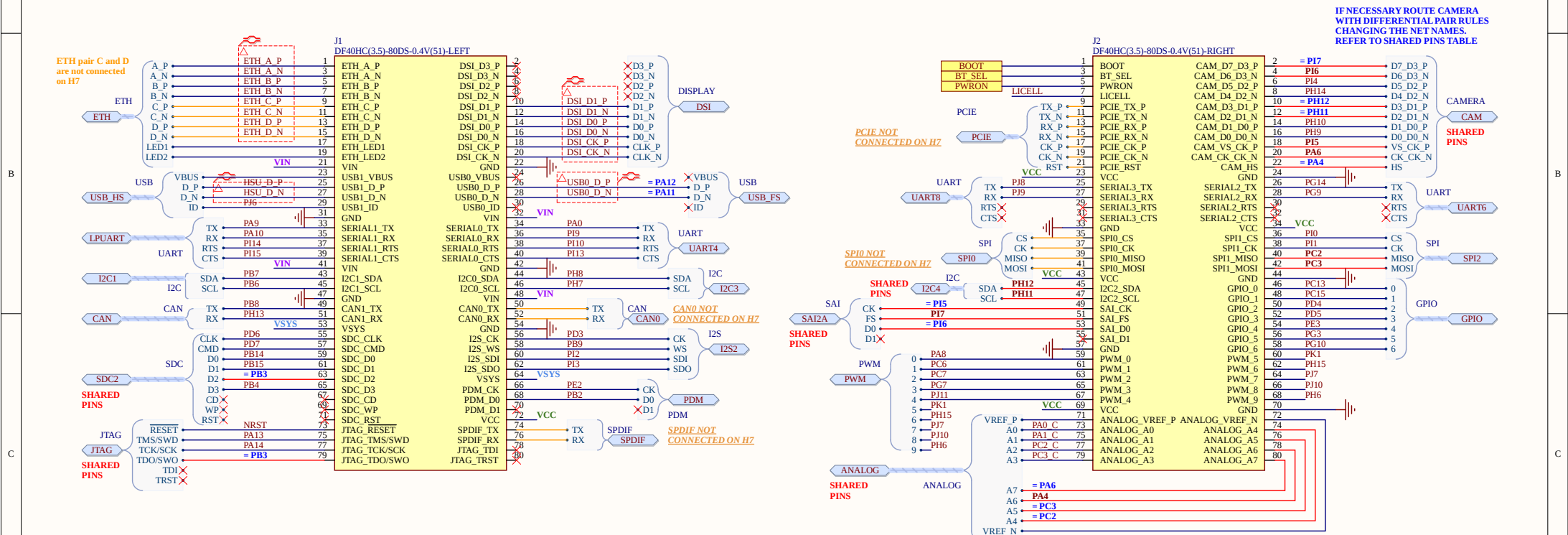
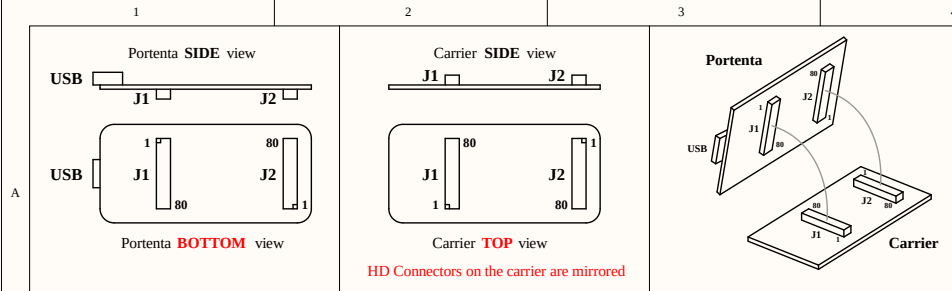
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SHARED PINS TABLE

NET	BUS 1	BUS 2
PB3	JTAG	SDC2
PHI1	CAM	I2C4
PHI2	CAM	I2C4
P15	CAM	SAI2A
P16	CAM	SAI2A
P17	CAM	SAI2A
PA4	CAM	ANALOG
PA6	CAM	ANALOG
PC2	ANALOG	SP12
PC3	ANALOG	SP12

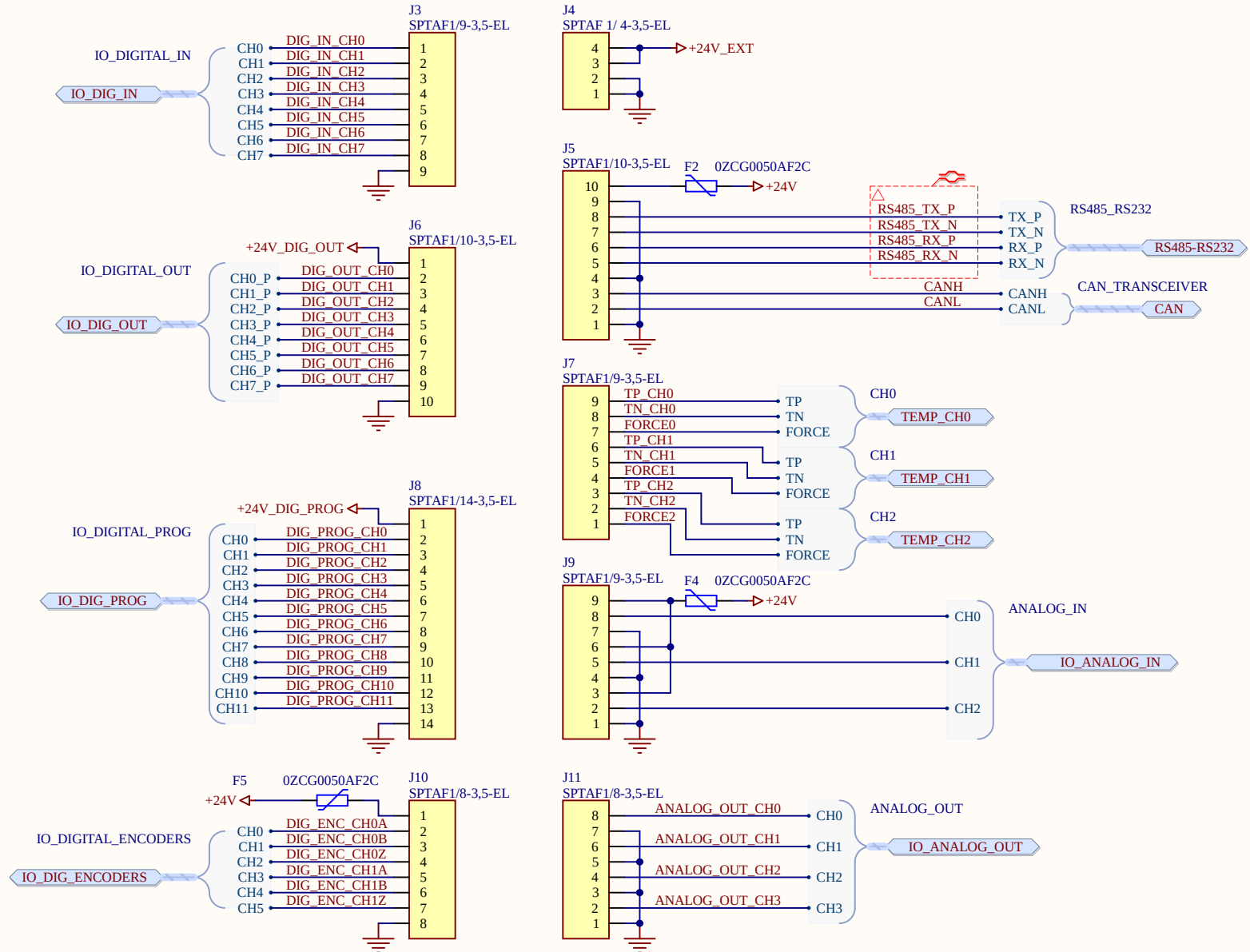
POWER NETS TABLE

NET	TYPE	RANGES	DESCRIPTION
 VIN	PORTENTA INPUT	4.1V to 6V.	Default 3.3V, PMIC (U10) programmable output.
 VCC	PORTENTA OUTPUT	1.1V to 3.3V in steps, max 1A.	Default 3.3V, PMIC (U10) programmable output.
 VSYS	PORTENTA RESERVED OUTPUT	RESERVED, DO NOT USE 3.5V to 4.2V, max 600mA.	Default 4.2V, PMIC (U10) programmable output which is also the input voltage of the bucks inside the PMIC itself.
 LICELL	PORTENTA INPUT	Coinc cell max 3.6V, max 46uA.	Max 4uA with PMIC (U10) in coin cell mode, max 46uA with PMIC in standby/suspend mode.

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Title: HD Connectors female			
ID: AKX00032	Revision: V1.1		
Date: 2021-05-11	Time: 15:10:53	Sheet 2 of 19	
File: HDConn_FEMALE.SchDoc		Author: S.Navaretti	RevAuthor: *



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Title: **MORSETTIERA**

ID: **AKX00032**

Revision: **V1.1**

Date: **2021-05-11** Time: **15:10:54**

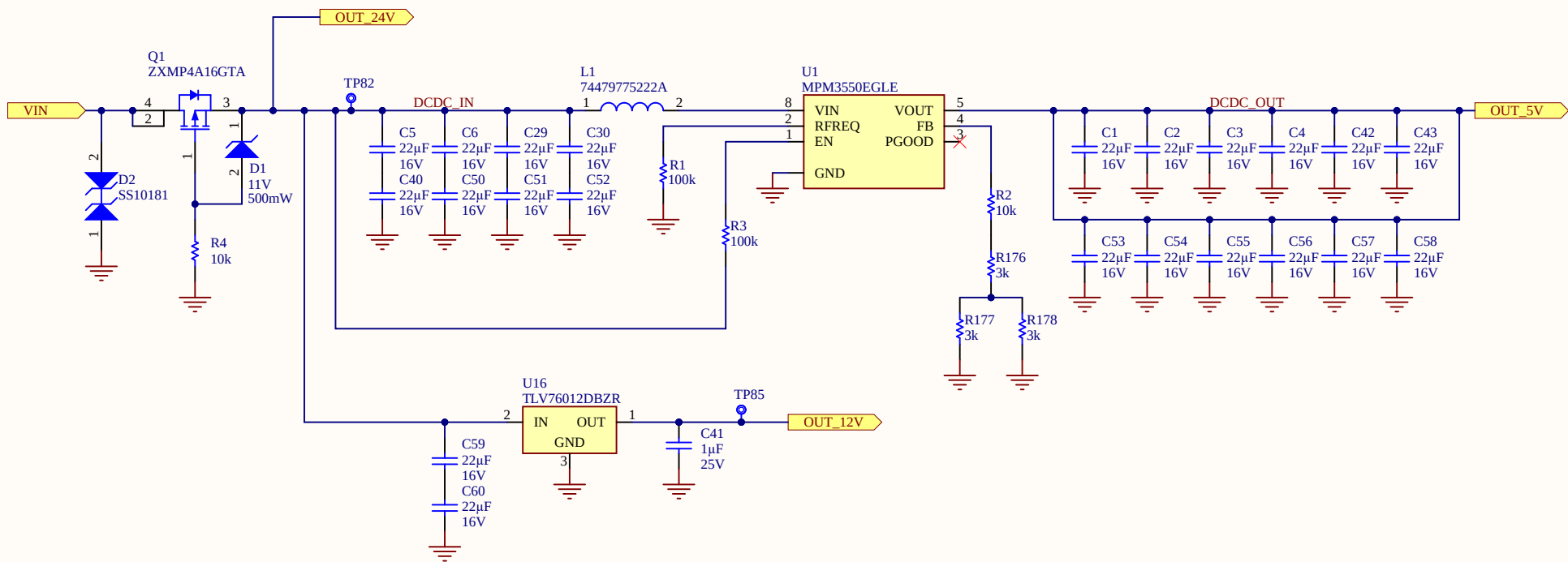
Sheet **3** of **19**

File: **MORSETTIERA.SchDoc**

Author: **S.Navaretti**

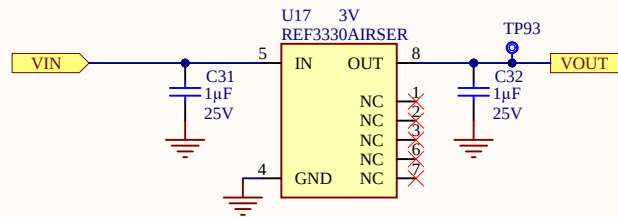
RevAuthor: **S.Navaretti**





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Title: POWER		 	
ID: AKX00032	Revision: V1.1		
Date: 2021-05-11	Time: 15:10:55	Sheet 4 of 19	
File: POWER.SchDoc		Author: S.Navaretti	RevAuthor: S.Navaretti



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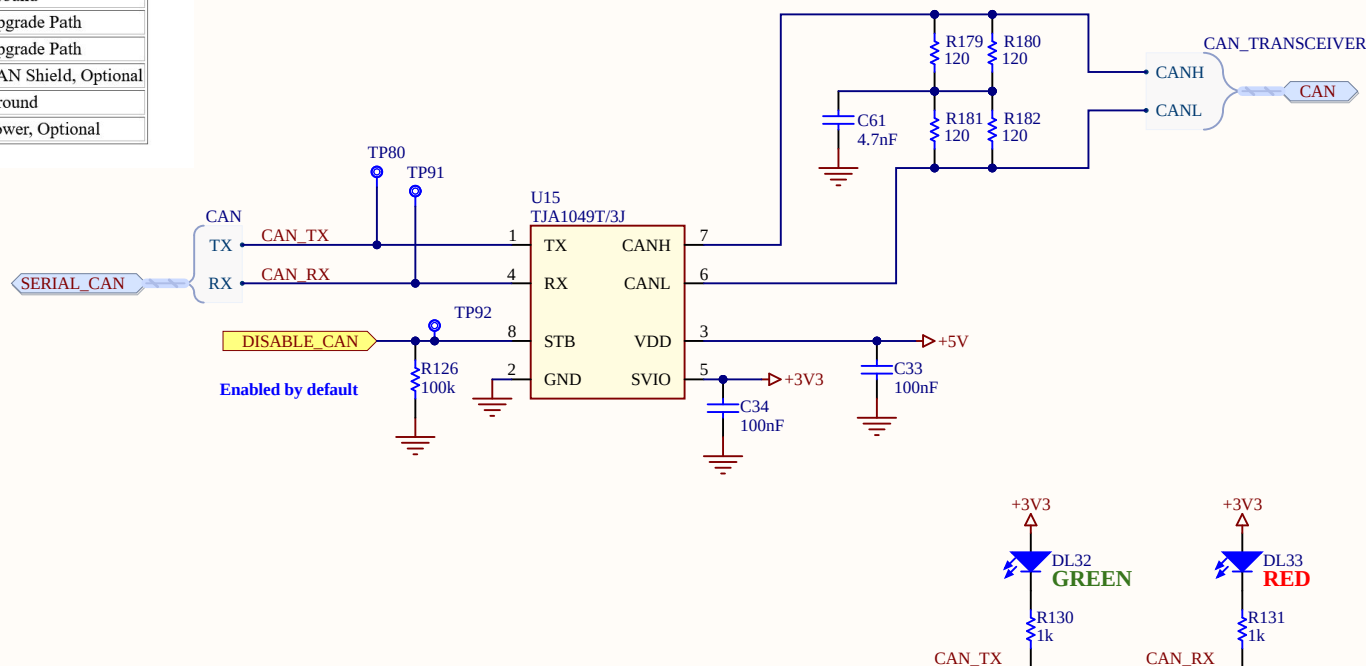
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Title: VOLTAGE REFERENCE				
ID: AKX00032	Revision: V1.1			
Date: 2021-05-11	Time: 15:10:56	Sheet 5 of 19	RevAuthor: S.Navaretti	
File: ADC_VOLTAGE_REFERENCE.SchDoc		Author: S.Navaretti		



RJ10, RJ45 CAN Bus PinOut

RJ45 Pin #	RJ10 Pin #	Signal name	Signal Description
1	2	CAN_H	Dominant High
2	3	CAN_L	Dominant Low
3	4	CAN_GND	Ground
4	-	Reserved	Upgrade Path
5	-	Reserved	Upgrade Path
6	-	CAN_SHLD	CAN Shield, Optional
7	-	CAN_GND	Ground
8	1	CAN_V+	Power, Optional



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Title: CAN

ID: AKX00032

Date: 2021-05-11 Time: 15:10:57

File: CAN.SchDoc

Revision: V1.1

Sheet 6 of 19

Author: S.Navaretti

RevAuthor: S.Navaretti



PIN DESCRIPTIONS

Pin	Name	RS-232	RS-485 Full Duplex	RS-485 Half Duplex
1				
2	GND		Ground	
3	T1OUT, B/Z	Transmitter 1 Output	Z Driver Neg Output	B/Z Neg Input/Output
4	T2OUT, A/Y	Transmitter 2 Output	Y Driver Pos Output	A/Y Pos Input/Output
5				
6	R1OUT	Receiver 1 Output	X	X
7	R2OUT, RO	Receiver 2 Output	Receiver TTL Output	Receiver TTL Output
8				
9				
10	SHDN		Low power shutdown mode when low	
11	SLEW		Data rate limited to 250kbps when low	
12	FD_TX_TERM	X	120Ω Y-Z termination enabled when both TERM and FD_TX_TERM are high	X
13	TERM	X	120Ω A-B termination enabled when high	
14	RS-485/RS-232	0	1	1
15	HALF/FULL	X	0	1
16				
17	GND		Ground	
18	R2IN, A	Receiver 2 Input	A Pos Receiver Input	X
19	R1IN, B	Receiver 1 Input	B Neg Receiver Input	X
20	RE	X	Receiver enabled when low	
21	T2IN, DE	Transmitter 2 Input	Driver enabled when high	
22	T1IN, DI	Transmitter 1 Input	Driver TTL Input	
23				
24				
25	V-		Charge pump negative supply, 0.1μF from ground	
26	C2-		Charge pump cap 2 negative lead	
27	C2+		Charge pump cap 2 positive lead, 0.1μF	
28	V+		Charge pump positive supply, 0.1μF to ground	
29	C1+		Charge pump cap 1 positive lead, 0.1μF	
30	VL		Logic Supply for TTL Inputs and Outputs, V _L = +1.65V to +5.5V or tie to V _{CC}	
31	VCC		Main Supply, V _{CC} = +3.0V to +5.5V, bypass to ground with 1.0μF	
32	C1-		Charge pump cap 1 negative lead	

TABLE 1: RS-232 TX TRUTH TABLE

INPUTS			OUTPUTS
SHDN	RS-485/RS-232	DI/T1IN, DE/T2IN	Z(B)/T1OUT, Y(A)/T2OUT
0	X	X	1/8th unit load
1	0	0	1
1	0	1	0
1	1	X	RS-485 Mode

TABLE 2: RS-232 RX TRUTH TABLE

INPUTS			OUTPUTS
SHDN	RS-485/RS-232	B/R1IN, A/R2IN	R1OUT, R2OUT
X	0	0	1
X	0	1	0
X	0	Inputs open	1
X	1	X	R1OUT High-Z, R2OUT in RS-485 Mode

TABLE 3: RS-485/422 TX TRUTH TABLE

INPUTS				OUTPUTS	
SHDN	RS-485/RS-232	DE/T2IN	DI/T1IN	Z(B)/T1OUT	Y(A)/T2OUT
0	X	X	X	1/8th unit load	1/8th unit load
1	1	0	X	1/8th unit load	1/8th unit load
1	1	1	0	1	0
1	1	1	1	0	1
X	0	X	X	RS-232 Mode	

TABLE 4: RS-485/422 RX TRUTH TABLE

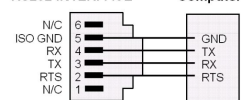
INPUTS				OUTPUT	
RS-485/RS-232	SHDN	HALF/FULL	RE	(A-B)	(Y-Z)
1	0	X	X	X	High-Z
1	1	0	0	X	1
1	1	0	0	> -50mV	X
1	1	0	0	< -200mV	0
1	1	1	0	X	> -50mV
1	1	1	0	X	< -200mV
1	1	1	0	X	Floating
1	1	X	1	X	X
0	X	X	X	X	X

TABLE 5: RS-485/422 TERMINATION TRUTH TABLE

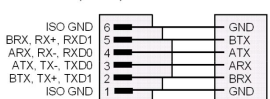
FD_TX_TERM	TERM	RS-485/RS-232	HALF/FULL	TX_TERM	RX_TERM
Pin 12	Pin 13	Pin 14	Pin 15	Pin 3-4	Pin 18-19
X	0	1	0	-	-
0	1	1	0	-	ON
1	1	1	0	ON	ON
X	0	1	1	-	-
X	1	1	1	ON	-
X	X	0	X	-	-

The DE and RE pins have no effect on the termination setting in any mode.

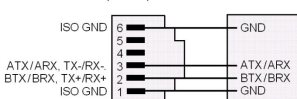
RS232 INTERFACE



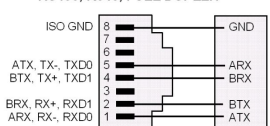
RS485, RJ11, FULL DUPLEX



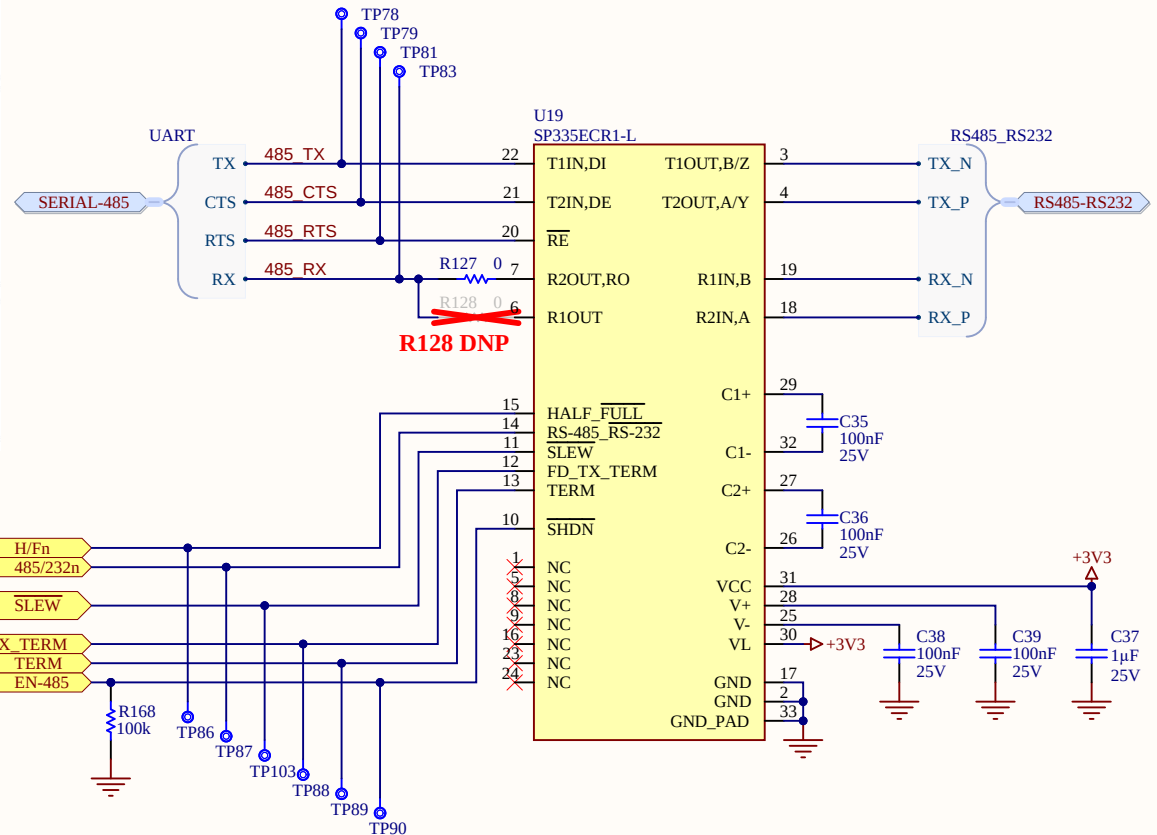
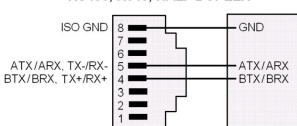
RS485, RJ11, HALF DUPLEX



RS485, RJ45, FULL DUPLEX



RS485, RJ45, HALF DUPLEX

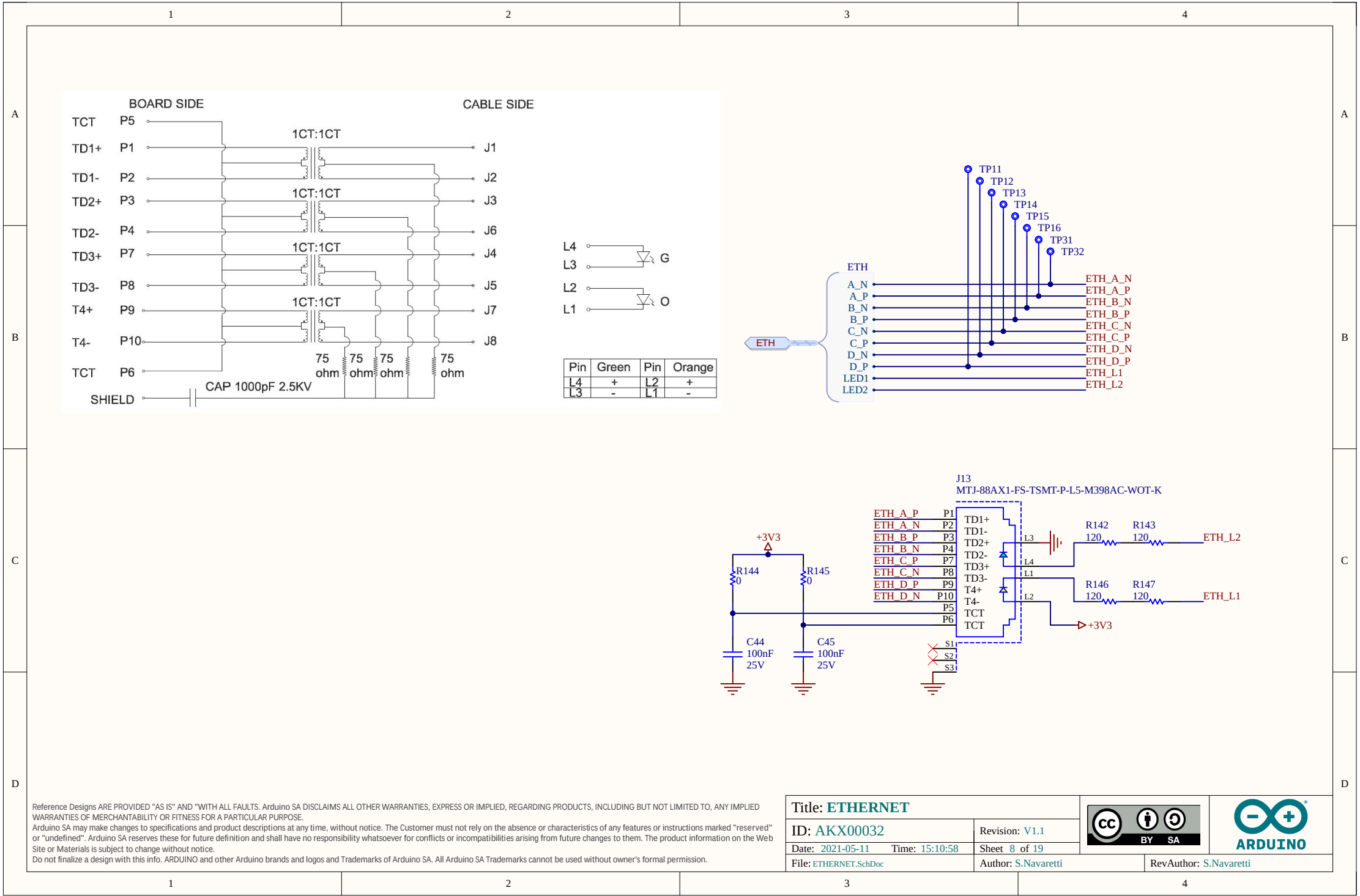


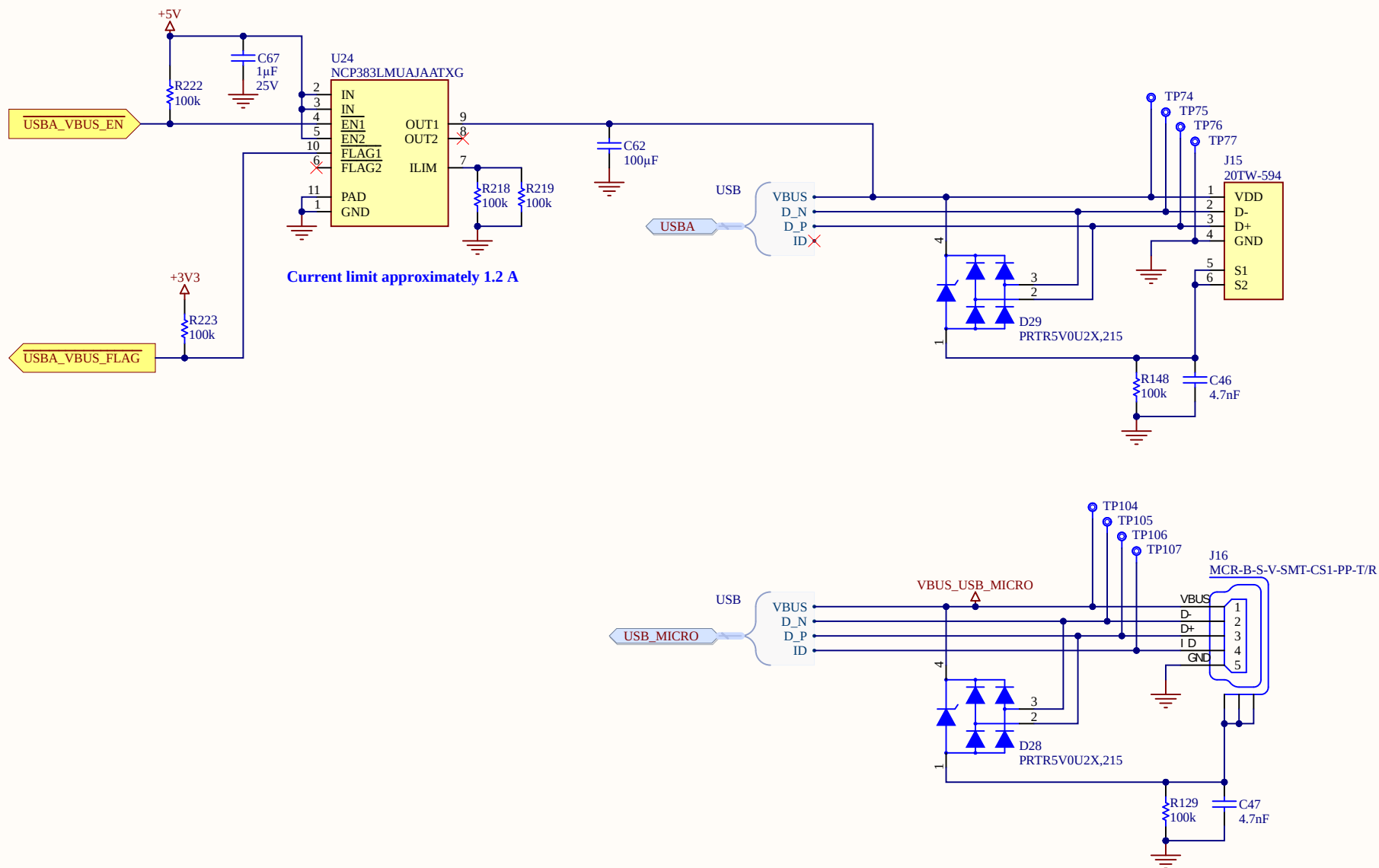
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Title: **RS485 / RS422 / RS232**ID: **AKX00032**Revision: **V1.1**Date: **2021-05-11** Time: **15:10:58**Sheet **7** of **19**File: **RS485_RS232.SchDoc**Author: **S.Navaretti**RevAuthor: **S.Navaretti**





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Title: **USB**

ID: **AKX00032**

Date: **2021-05-11** Time: **15:10:59**

File: **USB.SchDoc**

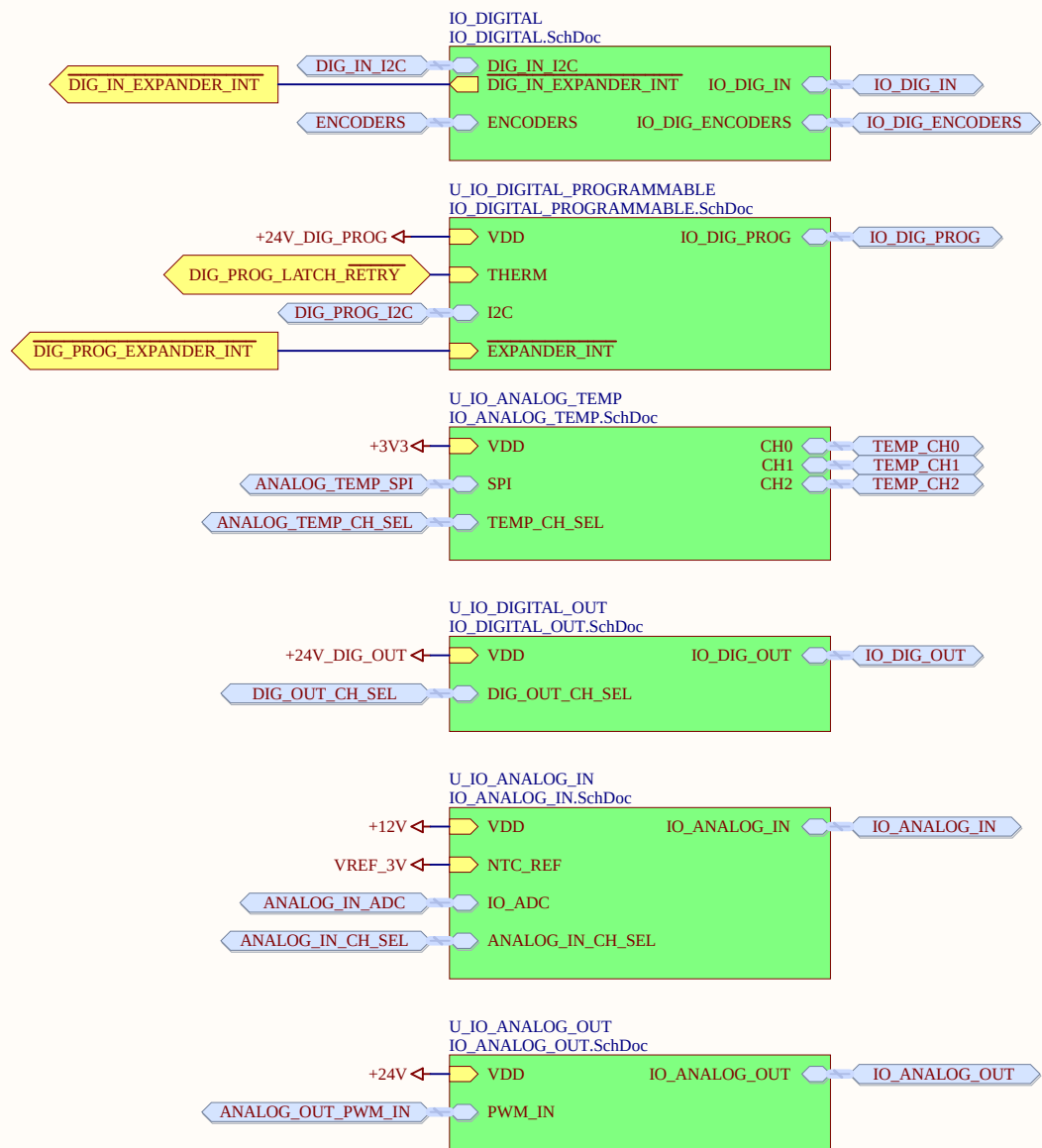
Revision: **V1.1**

Sheet **9** of **19**

Author: **S.Navaretti**

RevAuthor: **S.Navaretti**





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Title: **IO TOP**

ID: **AKX00032**

Revision: **V1.1**

Date: **2021-05-11**

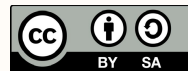
Time: **15:11:01**

Sheet **11 of 19**

File: **IO.SchDoc**

Author: **S.Navaretti**

RevAuthor: **S.Navaretti**



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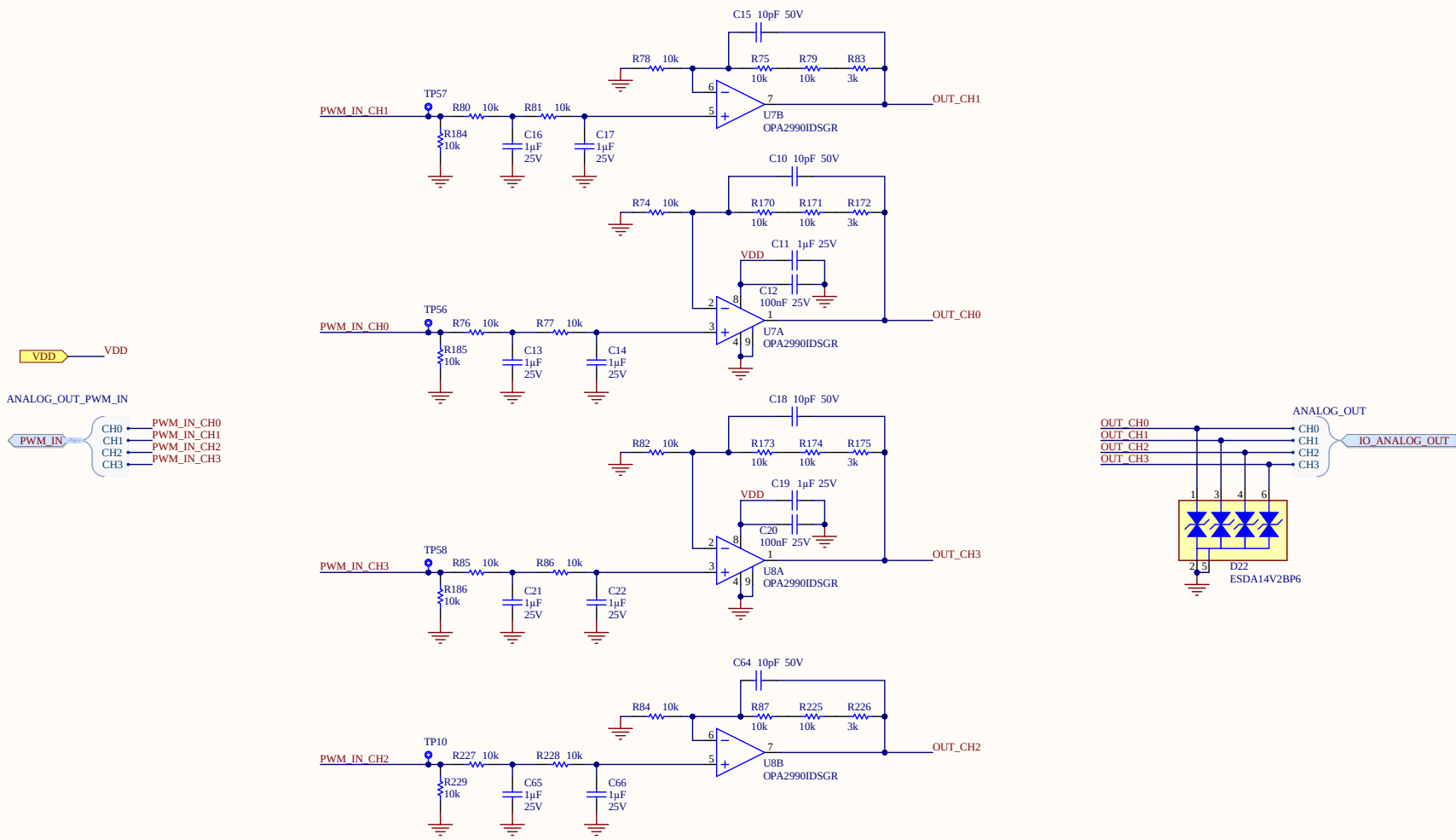
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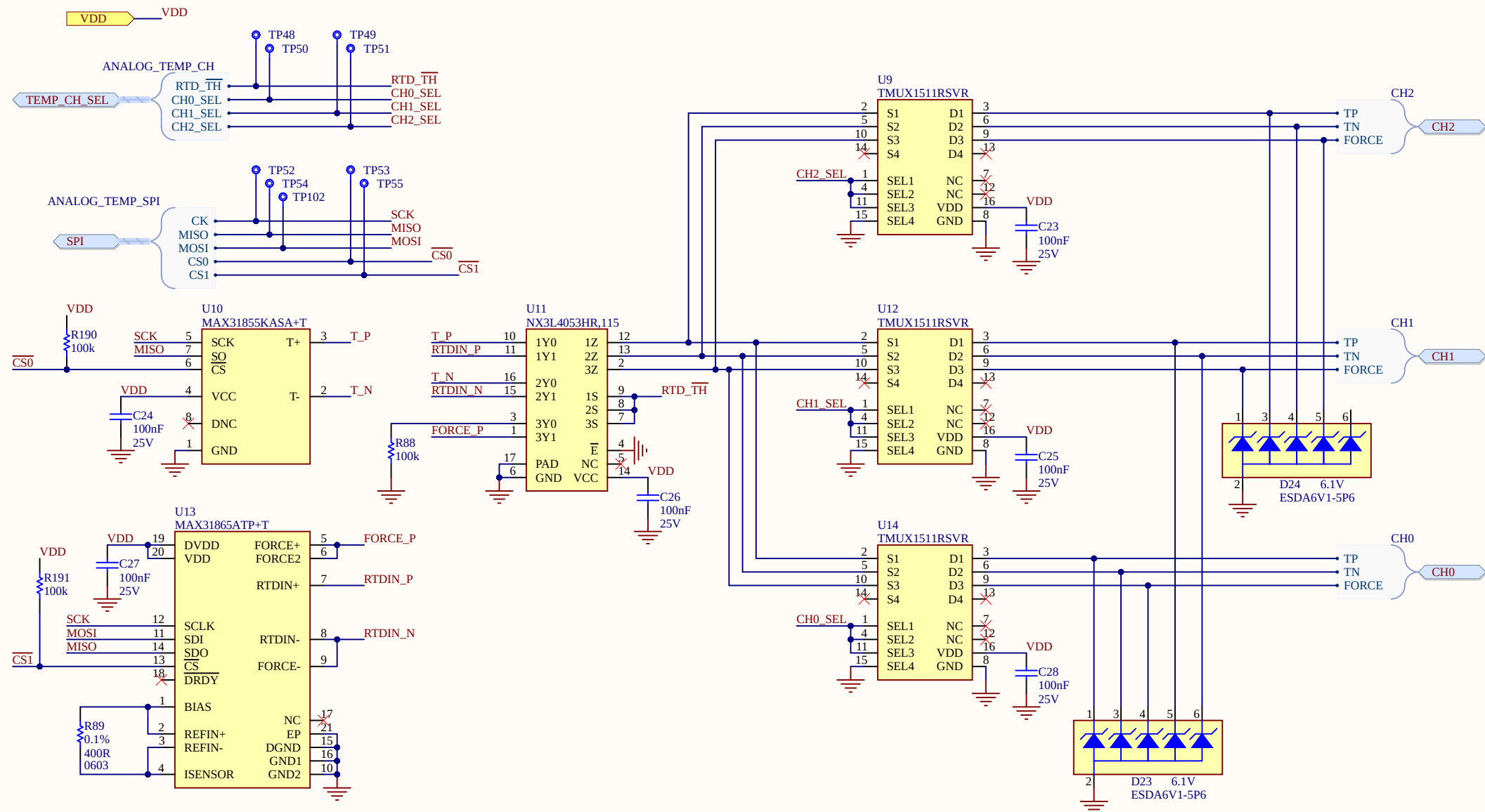
Title: ANALOG OUT			
ID: AKX00032	Revision: V1.1		
Date: 2021-05-11	Time: 15:11:03	Sheet 13 of 19	RevAuthor: S.Navaretti
File: IO_ANALOG_OUT.SchDoc		Author: S.Navaretti	

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Title: **ANALOG TEMP**

ID: **AKX00032**

Revision: **V1.1**

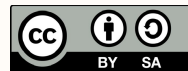
Date: **2021-05-11** Time: **15:11:04**

Sheet **14** of **19**

File: **IO_ANALOG_TEMP.SchDoc**

Author: **S.Navaretti**

RevAuthor: **S.Navaretti**

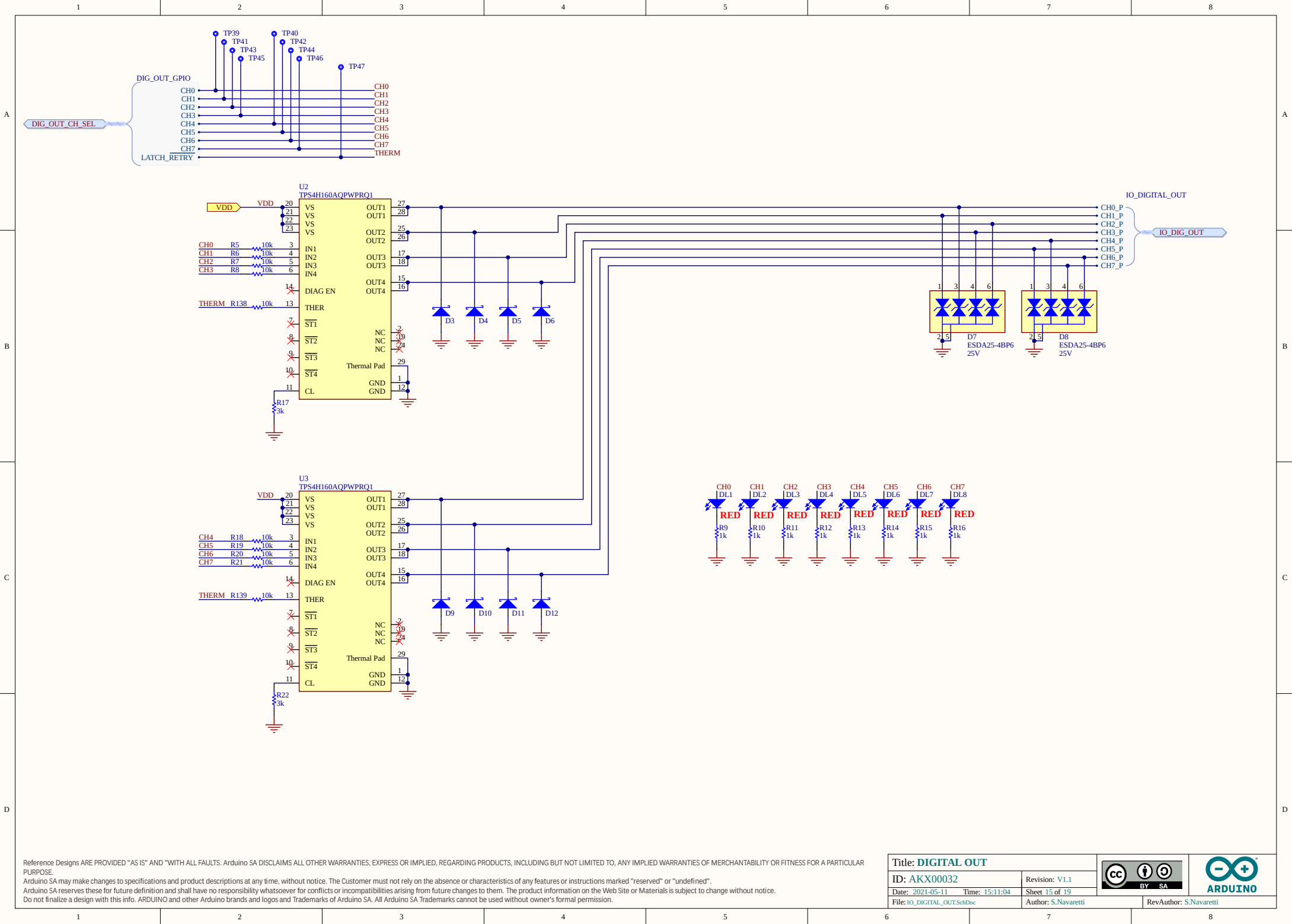


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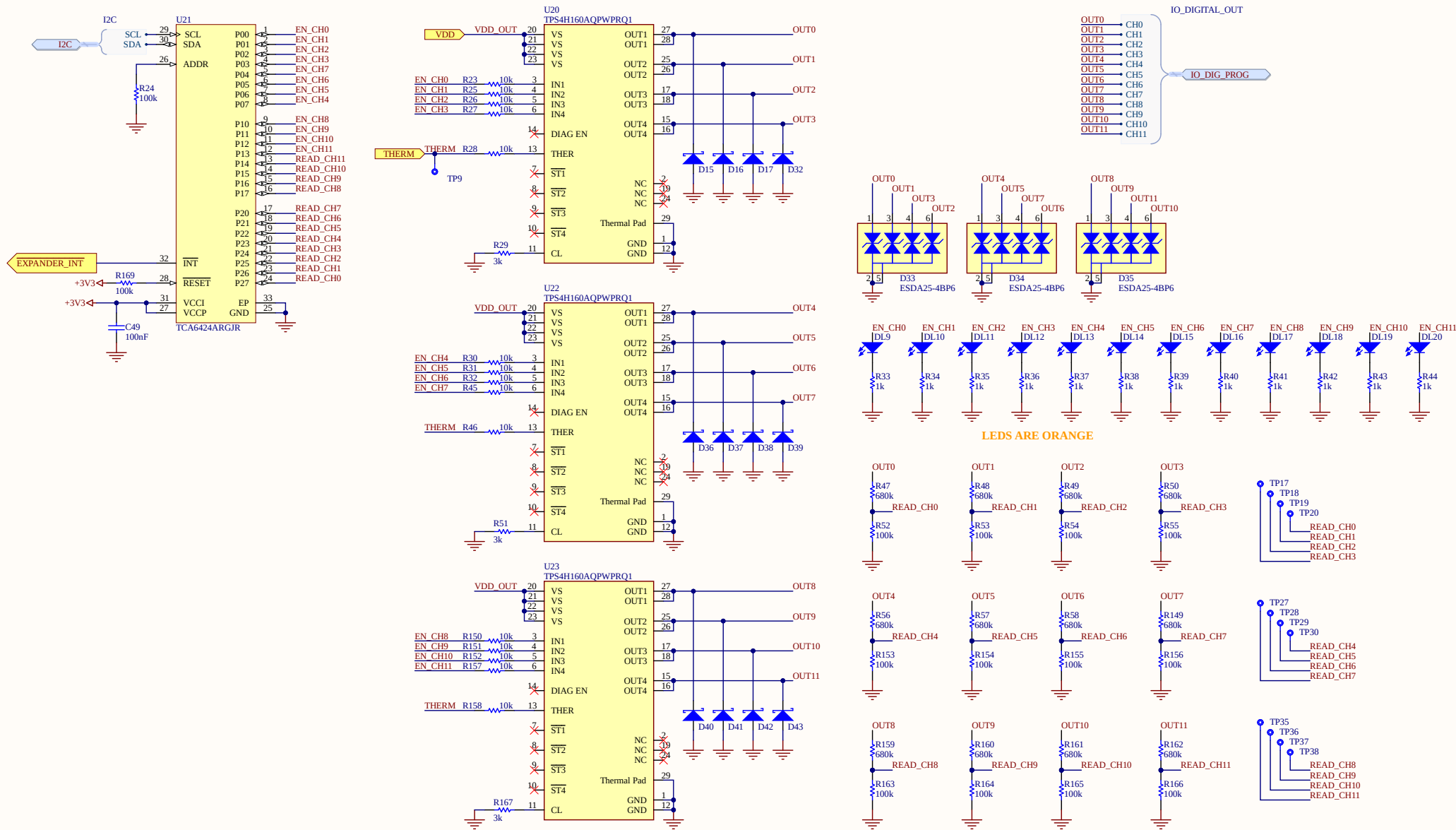
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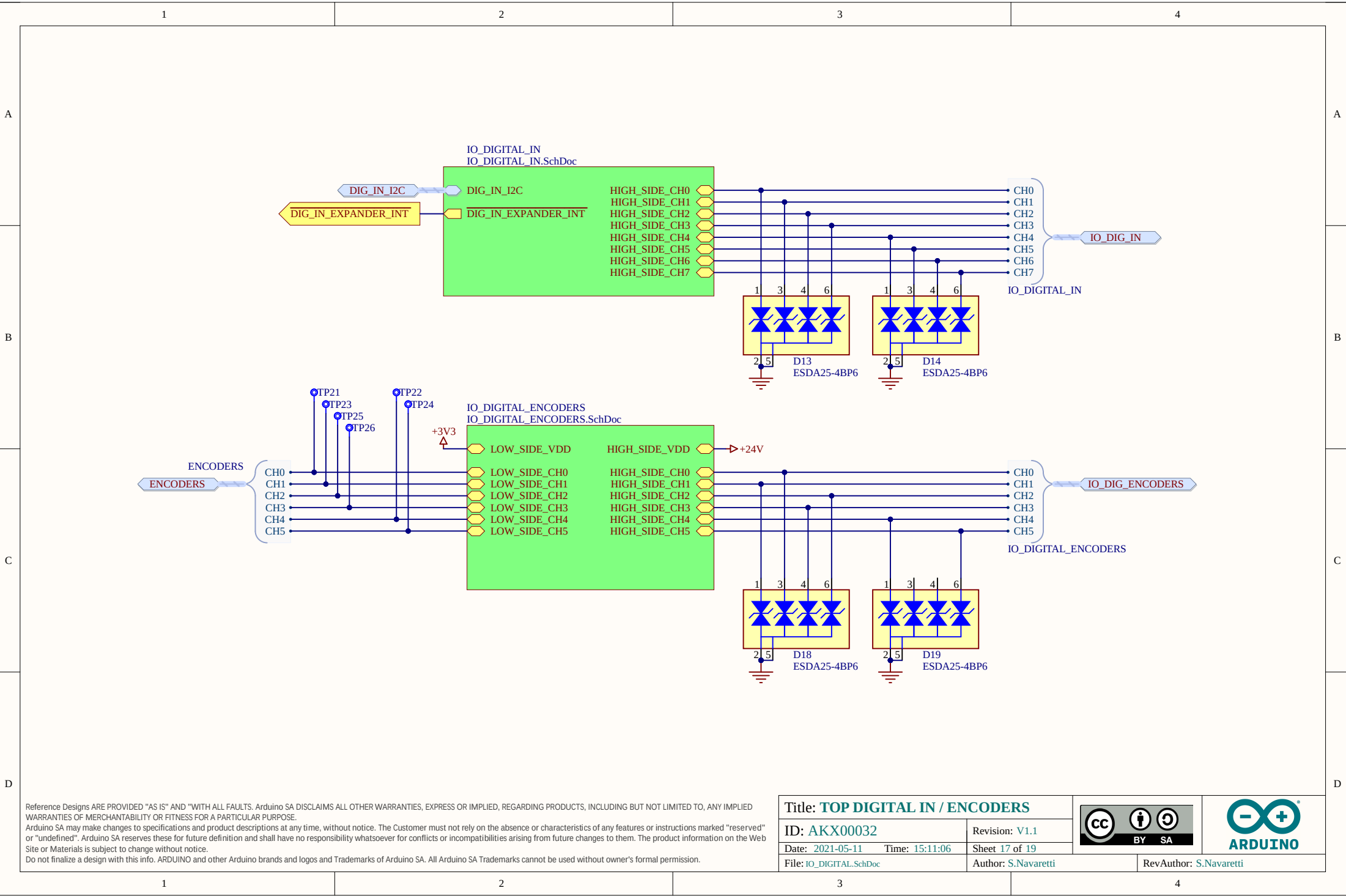
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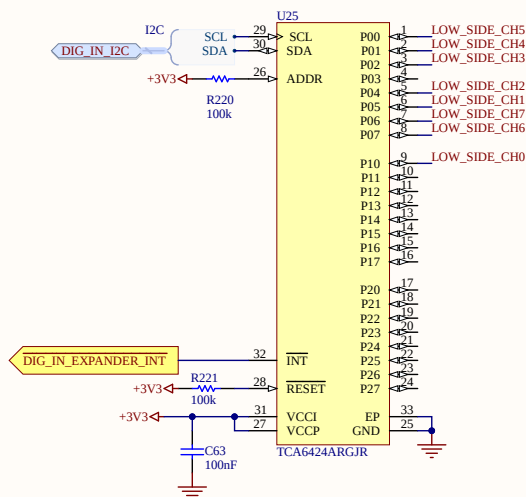
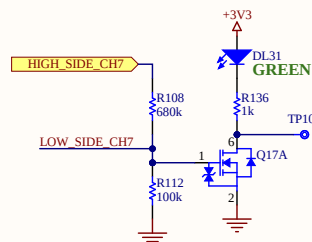
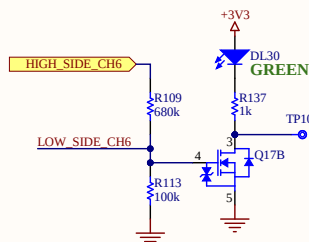
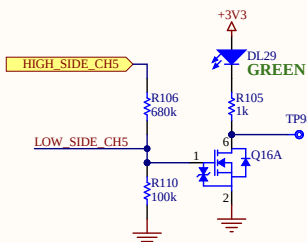
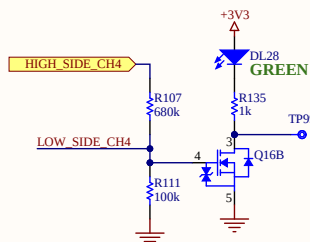
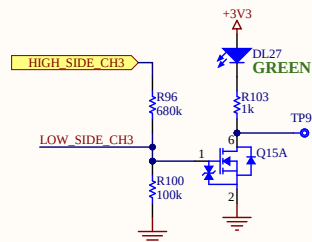
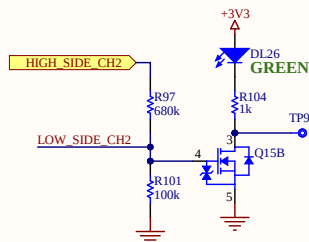
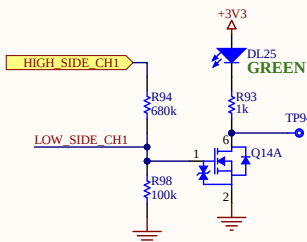
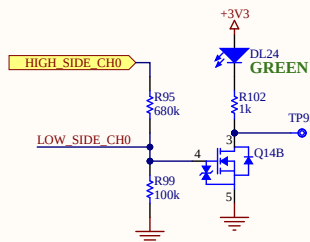




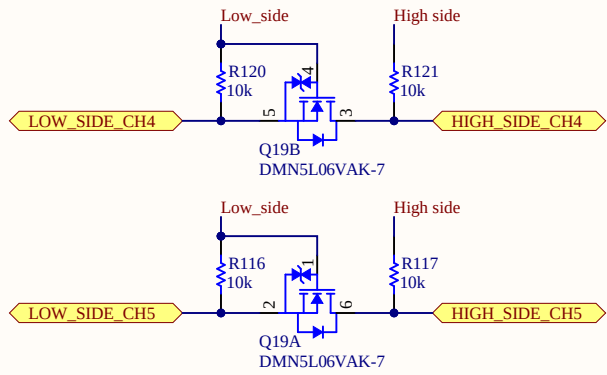
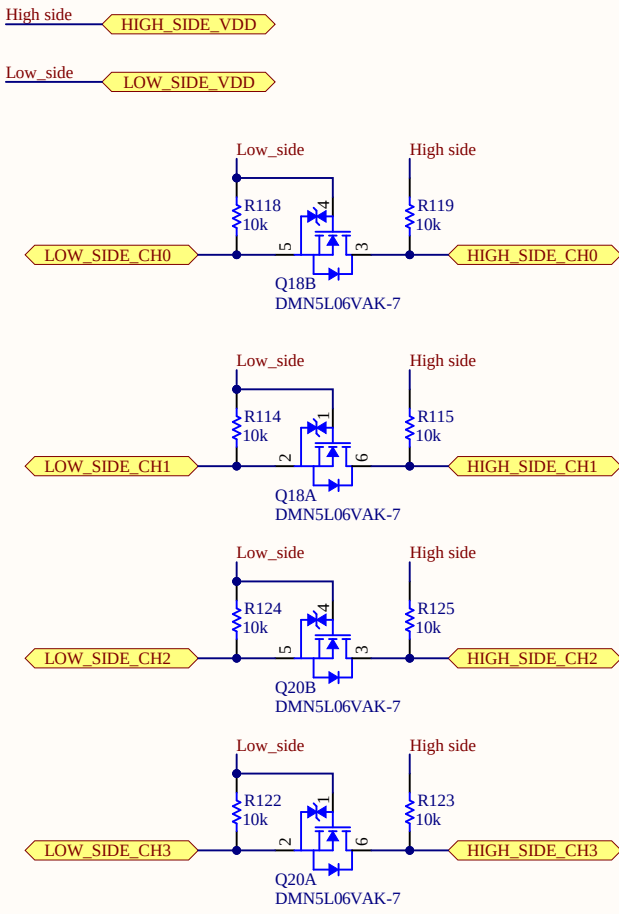
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Title: TOP DIGITAL IN / ENCODERS				
ID: AKX00032	Revision: V1.1			
Date: 2021-05-11	Time: 15:11:06	Sheet 17 of 19	RevAuthor: S.Navaretti	
File: IO_DIGITAL.SchDoc		Author: S.Navaretti		

LOW_SIDE_CH0 TP1
 LOW_SIDE_CH1 TP3
 LOW_SIDE_CH2 TP5
 LOW_SIDE_CH3 TP7
 LOW_SIDE_CH4 TP2
 LOW_SIDE_CH5 TP4
 LOW_SIDE_CH6 TP6
 LOW_SIDE_CH7 TP8



These pins should be set as INPUTS



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